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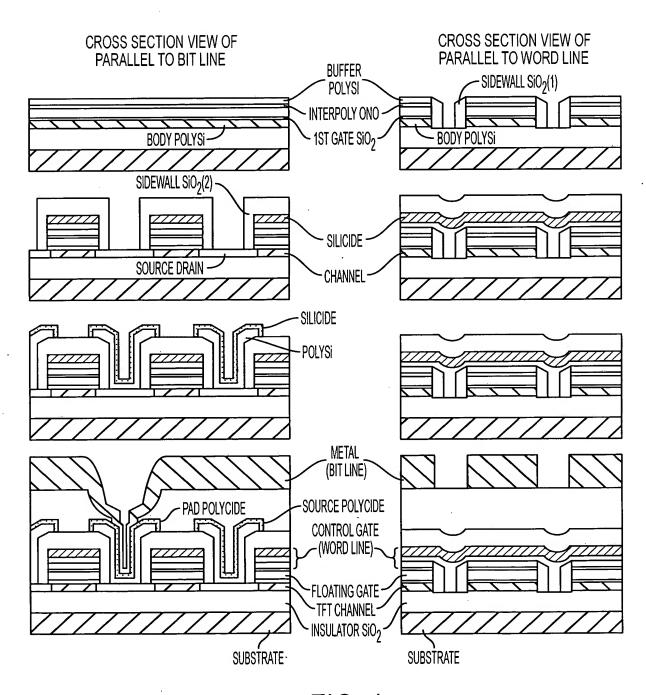
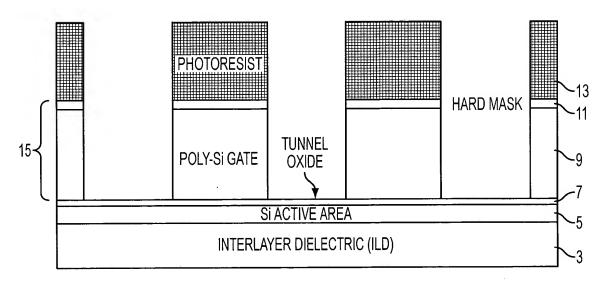


FIG. 1 PRIOR ART



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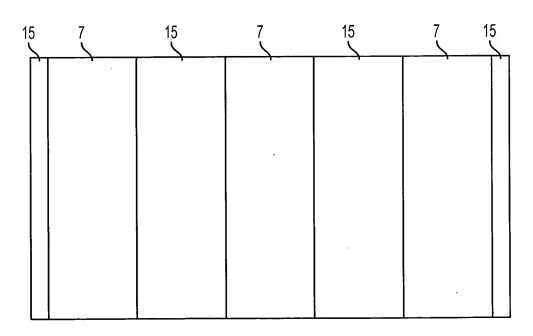


FIG. 3



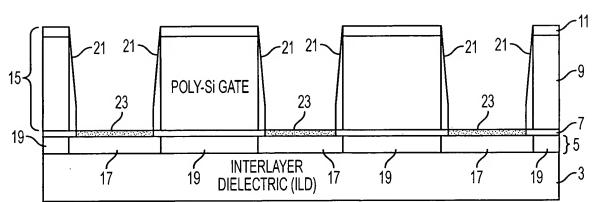


FIG. 4

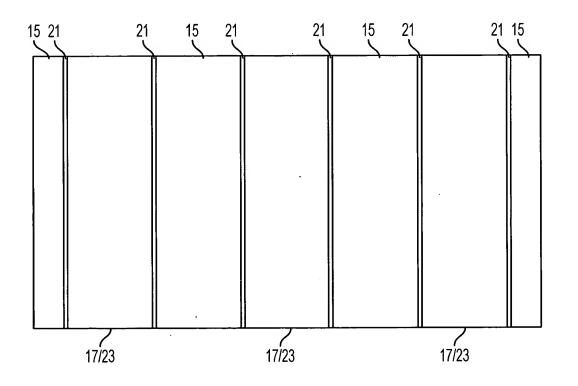


FIG. 5

MAY 1 L 2004 E

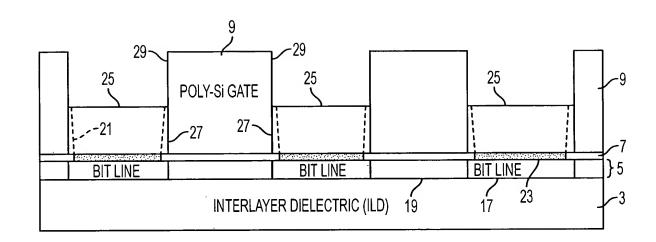


FIG. 6

MAY 1 & 2004 BY

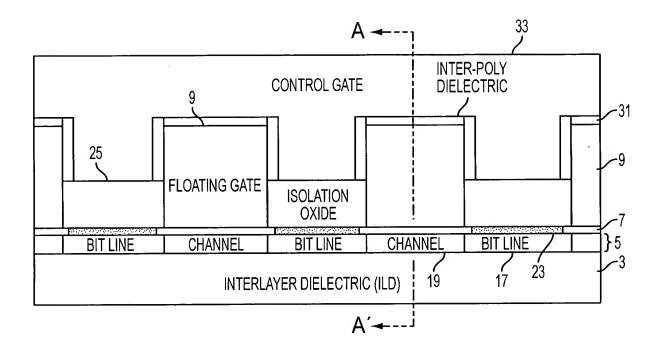


FIG. 7

Title: TWO MASK FLOATING GATE EEPROM
AND METHOD OF MAKING
Inventor(s): Ignr G. KOLIZNETSOV et al.

Inventor(s): Igor G. KOUZNETSOV et al. Appl. No.: 10/066,376



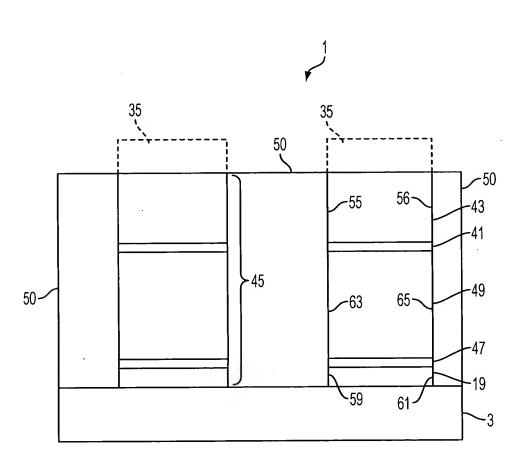


FIG. 8

MAY 1 L 2004 SE

17 49 17 49 17 49 43/53 57 57 57 43/53

FIG. 9

57



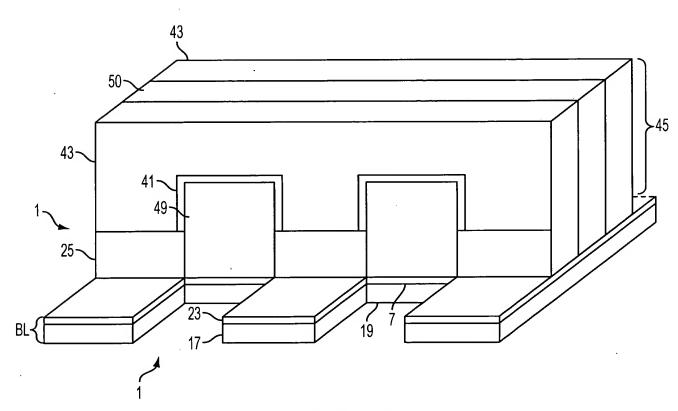
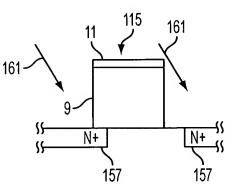


FIG. 10



INTER-POLY 143 DIELECTRIC **CONTROL GATE** 41 149 25 FLOATING GATE ISOLATION OXIDE 23 CHANNEL BIT LINE BIT LINE CHANNEL BIT LINE INTERLAYER DIELECTRIC (ILD) 17*i*157 17/157 19 151

FIG. 11



100



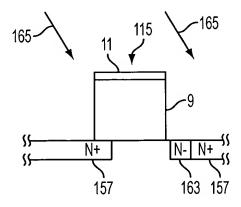


FIG. 13



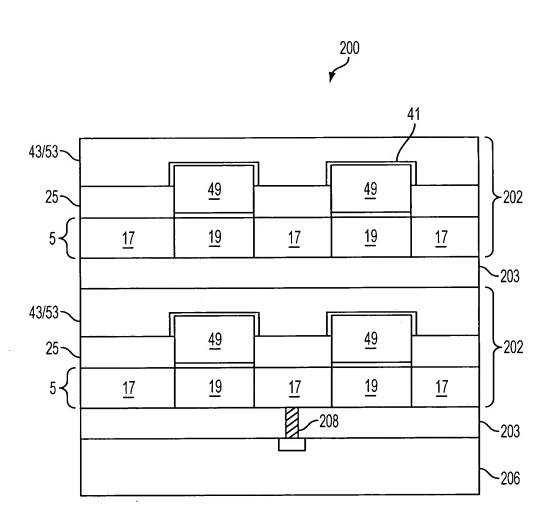


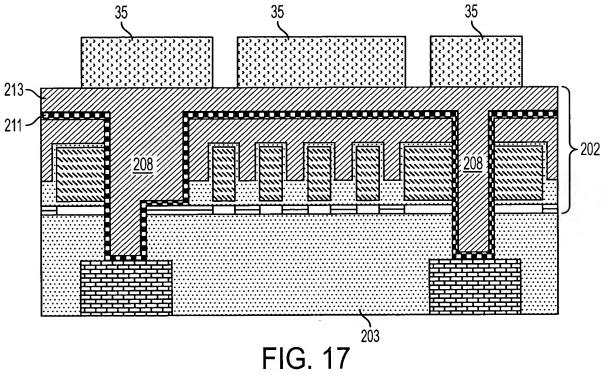
FIG. 14

Inventor(s): Igor G. KOUZNETSOV et al. Appl. No.: 10/066,376 209 209 209 33 31 -202 19::17::19::17::19: 203 202 202 or 206 or 206 FIG. 15 203

Title: TWO MASK FLOATING GATE EEPROM AND METHOD OF MAKING

FIG. 16





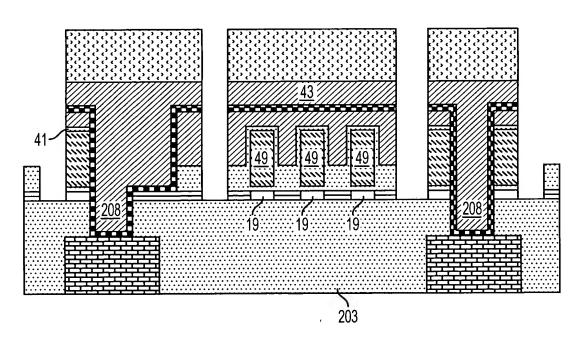


FIG. 18